IN THE CLAIMS

1. (Canceled)

2. (Canceled)

3. A method of multichannel analog/digital (A/D) conversion, in which in a first and second channel respectively in a first or second channel provision area a first and second analog signal awaiting conversion is sampled by a respective first and second S/H (Sample & Hold) element and the respectively stored sample value thereof is applied as a channel sample to a first and second input of an analog multiplexer for selection,

wherein the processing of the respective channel sample then takes place in a processing cycle of all channels by said channel sample being selected in the analog multiplexer by a digital selection control signal for the analog/digital conversion and provided as analog selection signal at an output of the analog multiplexer and, after the respective channel provision area, being converted in an analog/digital converter,

wherein an order of processing the channel sample detected in the respective first or second channel provision area , which channel sample is provided by the analog selection signal in an A/D conversion provision area and then converted by the A/D converter, is calculated and determined individually for each channel sample by a channel controller~~A method as claimed in claim 2~~,

wherein ~~the~~ calculations created in the channel controller for ~~the~~ an expiry of the multichannel analog/digital conversion are valid exclusively for detecting the channel samples in the first or second channel provision area.

_____wherein the detection of the channel sample present in the first or second channel provision area is respectively triggered by a first and second external detection signal-.

4. (Previously presented) A method as claimed in claim 3, wherein a multichannel analog/digital conversion that continues through the detection of the channel sample present as analog signal in the first and/or second channel provision area is initiated in the A/D conversion provision area by an external conversion request signal which thus deposits a conversion request in the channel controller .

5. (Previously presented) A method as claimed in claim 4, wherein additional data of the detected channel sample, which qualify an individual calculation of the time for processing a respectively detected channel sample in the channel controller , are notified to the channel controller with the triggering of the conversion request by the additional external conversion request signal .

6. (Previously presented) A method as claimed in claim 5, wherein the additional data, which are respectively notified to the channel controller with the detected channel sample upon triggering of the associated conversion request signal , are an initial priority date, an increase rate of the priority per unit time, and an overall and a minimum validity period.

7. (Previously presented) A method as claimed in claim 6, wherein the conversion request signals are fed to the channel controller together with the additional data on a data bus.

8. (Canceled)

9. (Currently amended) A method as claimed in claim 32, wherein all signal-influencing times which lead to a shortening of the validity of a channel sample compared to its individual sampling period within the first and/or second channel from the first and/or second S/H element to the A/D S/H element upstream of the A/D converter are combined to form an invalidity period and with their invalidity period form a configuration variable that influences the metrics.

10. (Currently amended) A method as claimed in claim 32, wherein one configuration variable that influences the metrics is the residual validity of a channel sample.

11. (Currently amended) A method as claimed in claim 32, wherein one configuration variable that influences the metrics is the minimum sampling period of a channel sample.

12. (Currently amended) A method as claimed in claim 32, wherein the residual validity of a channel sample, which results from the currently remaining validity period of a respective channel sample present as analog signal in the respective assembly defining the analog signal, is determined in the form of a realized integrator assigned to this analog signal, wherein the integrator initial value which represents the validity period that has passed is presently monitored and, if this value exceeds the representing value of the overall validity , expiry of the validity period is ascertained, and otherwise its difference

from the representing value of the overall validity is the representing value of the remaining validity period.

13. (Currently amended) A method as claimed in claim 32, wherein one configuration variable that influences the metrics is the randomly predefined priority of a channel sample.

14. (Currently amended) A method as claimed in claim 32, wherein the respectively currently remaining validity period of the output signals of all the assemblies defining the analog signals in the first and second channel provision area is known to the channel controller and the remaining validity period is continuously determined anew in advance, and in that the next signal processing step in the respective assembly defining the analog signal is thus triggered by the channel controller .

15. (Currently amended) A method as claimed in claim 32, wherein in the case of expiry of the validity period of one of the output signals of the assemblies defining the analog signals being determined by the channel controller in the first and second channel provision area , an error signal assigned to the respective output signal is output by the channel controller , or in the case of an available first S/H buffer memory or first further buffer memory or second S/H buffer memory or second further buffer memory these output signals are buffer-stored by means of a first buffer memory control signal or first further buffer memory control signal or second buffer memory control signal or second further buffer memory control signal-.

16. A method as claimed in claim ~~32~~ 31, wherein one configuration variable that influences the metrics is the buffer-storage that has taken place of a channel sample in a first and/or second S/H intermediate element and/or a first and/or second further buffer memory .

17.-26. (Canceled)

27. (New) A method of A/D conversion using a multi-channel A/D converter comprising a plurality of input channels, a channel multiplexer, a shared A/D converter, and a controller, the method comprising the steps of:

the controller dynamically controlling sample rates of the input channels in response to data provided to the controller via a conversion request bus;

sampling the input signals applied to the input channels in accordance with said sample rates to produce sampled input signals; and

performing A/D conversion of the sampled input signals using the shared A/D converter.

28. (New) The method of claim 27, comprising selecting a sample rate for each of the input channels from among multiple available sample rates.

29. (New) The method of claim 27, wherein the multiple available sample rates are binary-weighted.

30. (New) The method of claim 27, comprising:

triggering commencement of an A/D conversion process for a first signal applied to a first input channel in response to a first external triggering signal;

triggering commencement of an A/D conversion process for a first signal applied to a first input channel in response to a first external triggering signal;

the controller scheduling A/D conversion of a sample of the first signal in response to the first triggering signal and data provided to the controller via the conversion request bus; and

the controller scheduling A/D conversion of a sample of the second signal in response to the second triggering signal and data provided to the controller via the conversion request bus.

31. (New) The method of claim 27, comprising selectively buffering for a time within buffer storage at least one of:

input signals to the channel multiplexer; and

output signals of the channel multiplexer.

32. (New) A multi-channel A/D converter comprising:

a plurality of input channels;

a channel multiplexer coupled to the input channels;

a shared A/D converter coupled to the channel multiplexer; and

a controller coupled to the input channels and to the shared A/D converter;

wherein the controller dynamically controls sample rates of the input channels in response to data provided to the controller via a conversion request bus.

33. (New) The apparatus of claim 32, wherein the controller selects a sample rate for each of the input channels from among multiple available sample rates.

34. (New) The apparatus of claim 33, wherein the multiple available sample rates are binary-weighted.

35. (New) The apparatus of claim 32, wherein the controller:

triggers commencement of an A/D conversion process for a first signal applied to a first input channel in response to a first external triggering signal;

triggers commencement of an A/D conversion process for a first signal applied to a first input channel in response to a first external triggering signal;

schedules A/D conversion of a sample of the first signal in response to the first triggering signal and data provided to the controller via the conversion request bus; and

schedules A/D conversion of a sample of the second signal in response to the second triggering signal and data provided to the controller via the conversion request bus.

36. (New) The apparatus of claim 32, comprising buffers for selectively buffering for a time within buffer storage at least one of:

input signals to the channel multiplexer; and

output signals of the channel multiplexer.